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June 2014

# FDMA420NZ

## Single N-Channel 2.5V Specified PowerTrench<sup>®</sup> MOSFET 20V, 5.7A, 30mΩ

### General Description

This Single N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench process to optimize the  $R_{DS(on)}$  @  $V_{GS}=2.5V$  on special MicroFET leadframe.

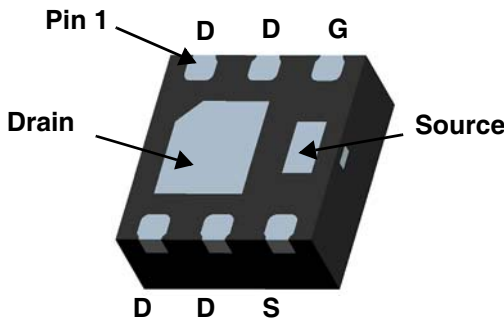
### Applications

- Li-Ion Battery Pack

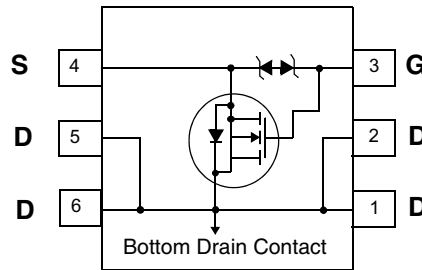


### Features

- $R_{DS(on)}$  = 30mΩ @  $V_{GS} = 4.5 V, I_D = 5.7A$
- $R_{DS(on)}$  = 40mΩ @  $V_{GS} = 2.5 V, I_D = 5.0A$
- Low Profile-0.8mm maximum-in the new package MicroFET 2x2 mm
- HBM ESD protection level > 2.5kV typical (Note 3)
- Free from halogenated compounds and antimony oxides
- RoHS Compliant



MicroFET Bottom View 2X2



### Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	20	V
$V_{GSS}$	Gate-Source Voltage	±12	V
$I_D$	Drain Current -Continuous (Note 1a) -Pulsed	5.7	A
		24	
$P_D$	Power dissipation (Steady State) (Note 1a) (Note 1b)	2.4	W
		0.9	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	145	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
420	FDMA420NZ	7"	8 mm	3000 units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$B_{VDSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	20			V
$\frac{\Delta B_{VDSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$ , Referenced to $25^\circ\text{C}$		12		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16V, V_{GS} = 0V$			1	$\mu A$
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 12V, V_{DS} = 0V$			$\pm 10$	$\mu A$

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.6	0.83	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\mu A$ , Referenced to $25^\circ\text{C}$		-3.1		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5V, I_D = 5.7A$		16.8	30	m $\Omega$
		$V_{GS} = 4.0V, I_D = 5.7A$		17.3	31	
		$V_{GS} = 3.1V, I_D = 5.0A$		18.9	33	
		$V_{GS} = 2.5V, I_D = 5.0A$		21.2	40	
		$V_{GS} = 4.5V, I_D = 5.7A, T_J = 150^\circ\text{C}$		24.8	44	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5V, I_D = 5.7A$		28.3		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 10V, V_{GS} = 0V, f = 1.0\text{MHz}$		701	935	pF
$C_{oss}$	Output Capacitance			163	220	pF
$C_{rss}$	Reverse Transfer Capacitance			125	190	pF
$R_G$	Gate Resistance	$f = 1.0\text{MHz}$		1.92		$\Omega$

**Switching Characteristics** (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GEN} = 6\Omega$		9.8	20	ns
$t_r$	Turn-On Rise Time			8.6	18	ns
$t_{d(off)}$	Turn-Off Delay Time			21.5	43	ns
$t_f$	Turn-Off Fall Time			8.6	18	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10V, I_D = 5.7A, V_{GS} = 4.5V$		8.8	12	nC
$Q_{gs}$	Gate-Source Charge			0.9	2	nC
$Q_{gd}$	Gate-Drain Charge			2.4	4	nC

**Drain-Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current			2.0	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0V, I_S = 2.0A$	0.69	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 5.7A$		20	ns
$Q_{rr}$	Diode Reverse Recovery Charge	$di/dt = 100A/\mu s$		5	nC

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.



a. 52  $^\circ\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 145  $^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu s$ , Duty Cycle < 2.0%.

3. The diode connected between the gate and the source serves only as protection against ESD. No gate overvoltage rating is implied.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

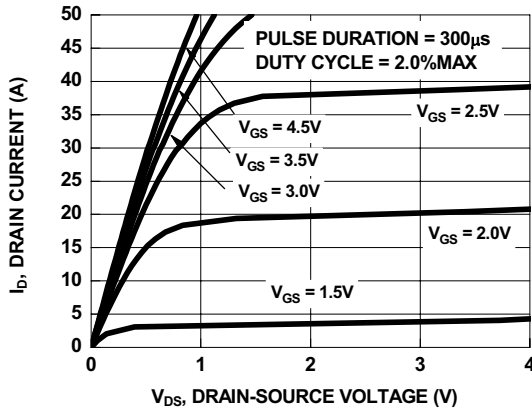


Figure 1. On Region Characteristics

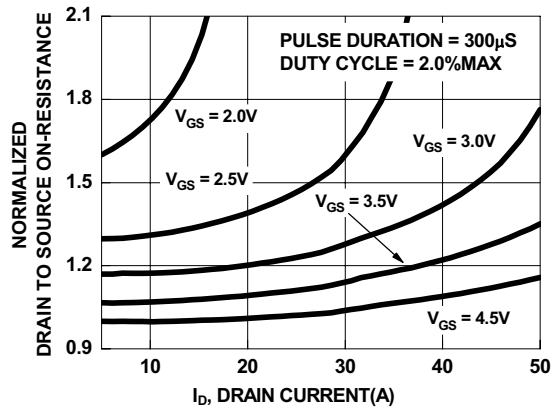


Figure 2. On-Resistance vs Drain Current and Gate Voltage

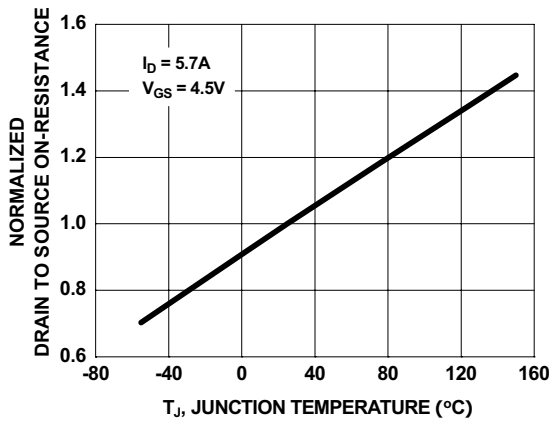


Figure 3. Normalized On Resistance vs Junction Temperature

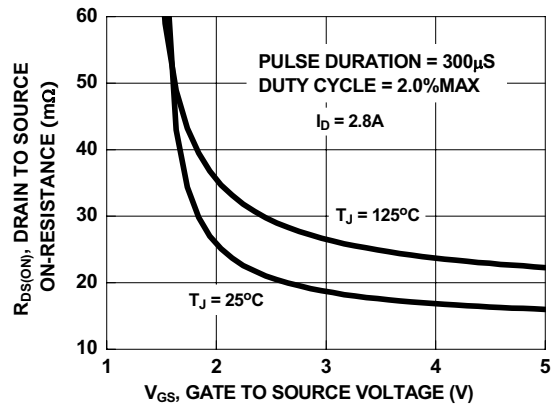


Figure 4. On-Resistance vs Gate to Source Voltage

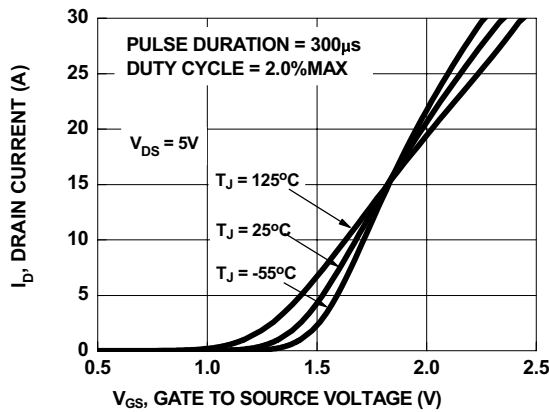


Figure 5. Transfer Characteristics

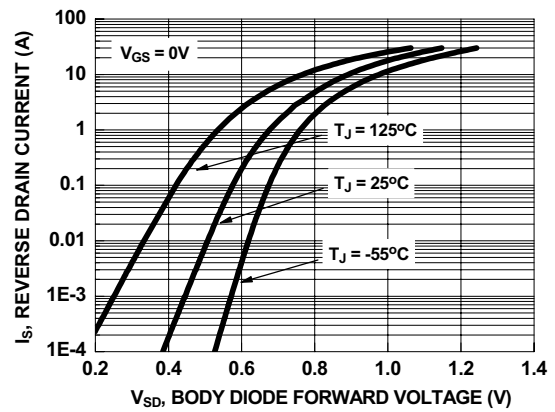


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

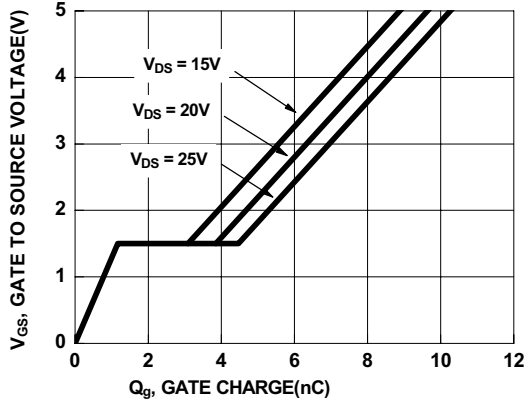


Figure 7. Gate Charge Characteristics

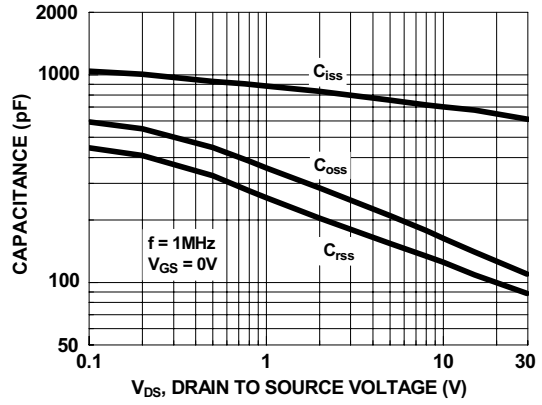


Figure 8. Capacitance vs Drain to Source Voltage

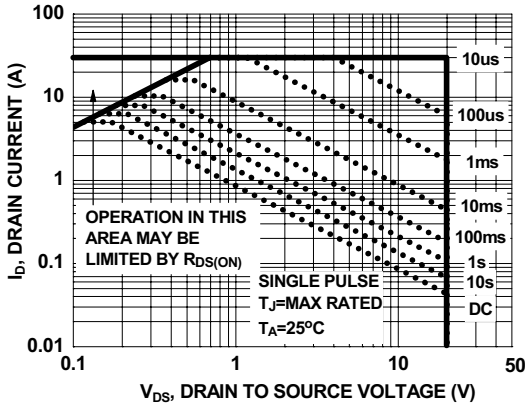


Figure 9. Forward Bias Safe Operating Area

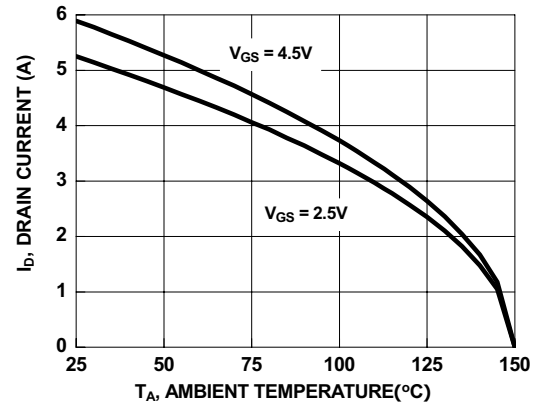


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

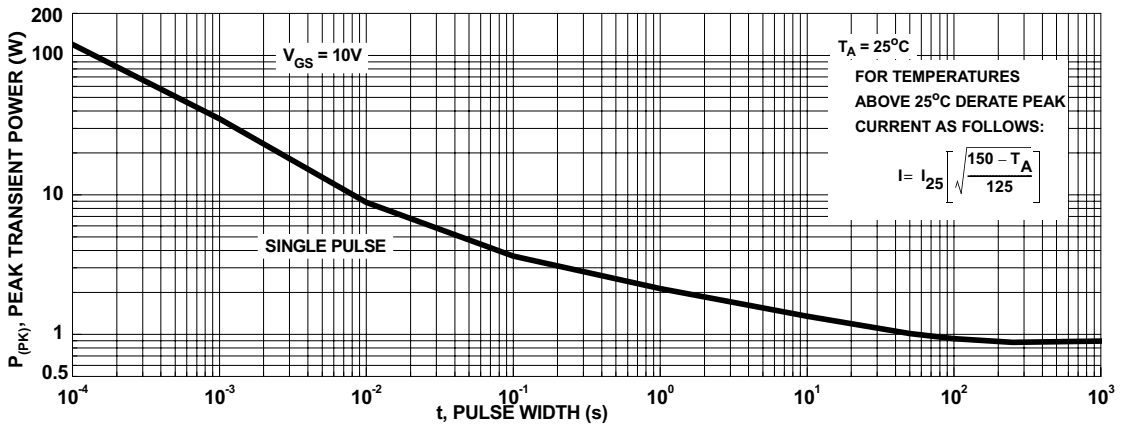


Figure 11. Single Pulse Maximum Power Dissipation

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

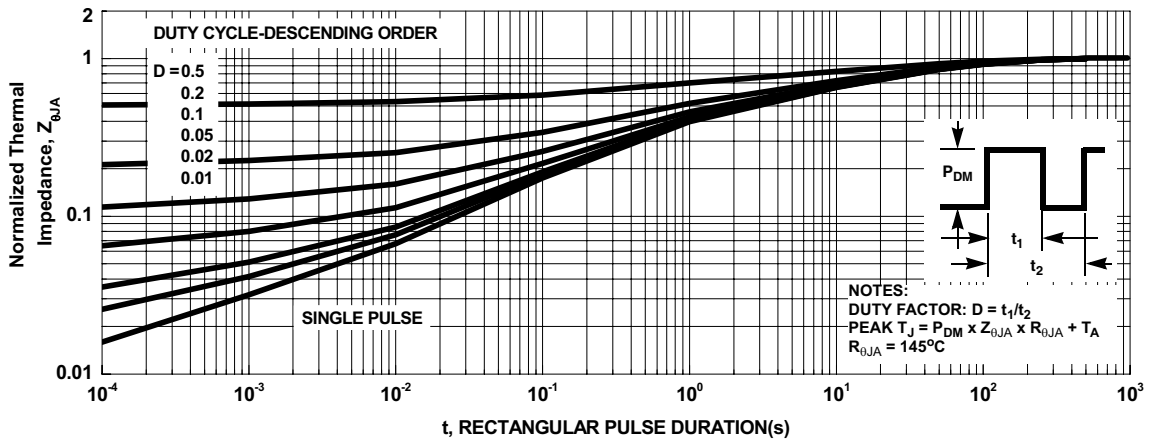
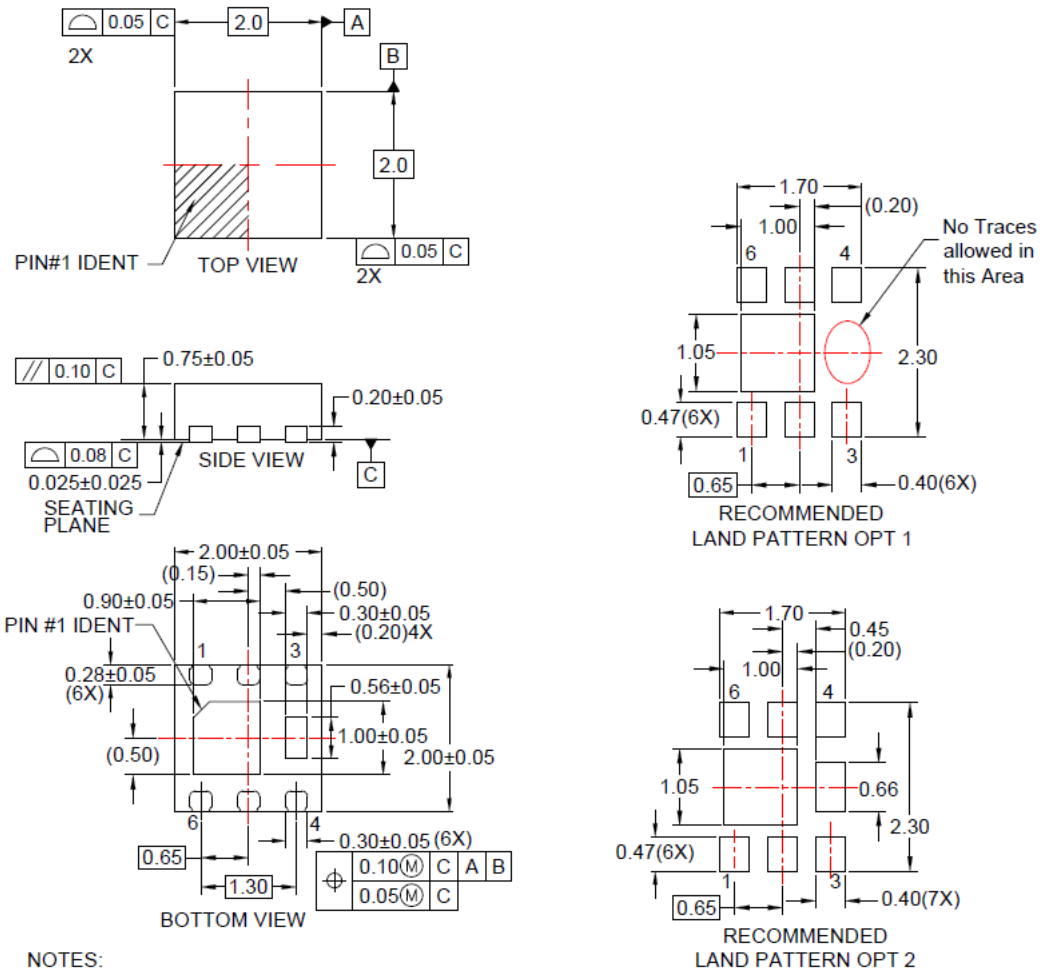


Figure 12. Transient Thermal Response Curve

Dimensional Outline and Pad Layout



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP06Rev4.








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